NCP2705

Product Preview

Audio Management Integrated Circuit with 2.8 W Class D and LongPlay True Ground Headphone Amplifier with Common Mode Sense

The NCP2705 is a cost effective audio subsystem designed for portable application such as mobile phones. It has been designed to cover the power audio requirements in portable equipment: including a high fidelity class D speaker amplifier and a Class G equivalent LongPlay true ground headset amplifier. This patented headset amplifier circuitry allows the removal of the bulky output capacitors and minimize audio playback current consumption with the minimum external component. In addition user can set the output swing to have enough output dynamic even when a damping resistor is added.

Through a flexible I^{2}C interface, NCP2705 can support both single ended and differential types of analog input signal. In both cases, it offers a zero pop noise signature. The same interface allows a user defined architecture with an input control, highly accurate gain setting capability from −60 dB to +12 dB (0 dB for the LS) and output control. In addition NCP2705 offers the possibility to reduce the EMI perturbation by lowering the rise and fall times of the Class D outputs (software programmable). The Loudspeaker amplifier includes also an AGC which performs two functions: limiter and non−clipping.

Features

- Flexible MUX Capability and Volume Control
  - Separated Mixer Control Between Louspeaker and Headset
  - Support Either Differential or Single−Ended Input
- High Sound Quality
  - −100 dB PSRR on Headset Amplifier
  - −80 dB PSRR On Loudspeaker Amplifier
  - 0.02% THD+N at 1 kHz on Headset Amplifier
  - 0.08% THD+N at 1 kHz on Loudspeaker Amplifier
- Low EMI Filterless Class D Loudspeaker Amplifier, Programmable High Efficiency or Low EMI Mode
- Programmable AGC: Non−Clipping or Power limit (Loudspeaker Output)
- Long Play True Ground Headset Amplifier, Programmable Output Swing (up to 5 V_{PP}) with Common Mode Sense
- I^{2}C Control and Software Shutdown
- No Pop and Click Noise
- TDMA Noise Free
- Thermal and Short−Circuit Protection
- 20−Bump Chip Scale Package (2.5 x 2.0 mm)
- This is a Pb−Free Device

Typical Applications

- Cellular Phones
- Portable Media Player

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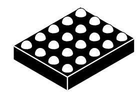
MARKING DIAGRAM



20 PIN CSP
FC SUFFIX
CASE 499BH

NCP2705
AYWW
▪

NCP2705	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

PINOUT

A1 IN2B	A2 IN1B	A3 HSR	A4 HSL	A5 PVM
B1 IN2A	B2 IN1A	B3 GND	B4 COM	B5 C1N
C1 I2CREF	C2 GND	C3 SCL	C4 SDA	C5 GND
D1 LPN	D2 PVDD	D3 LPP	D4 HSVDD	D5 C1P

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

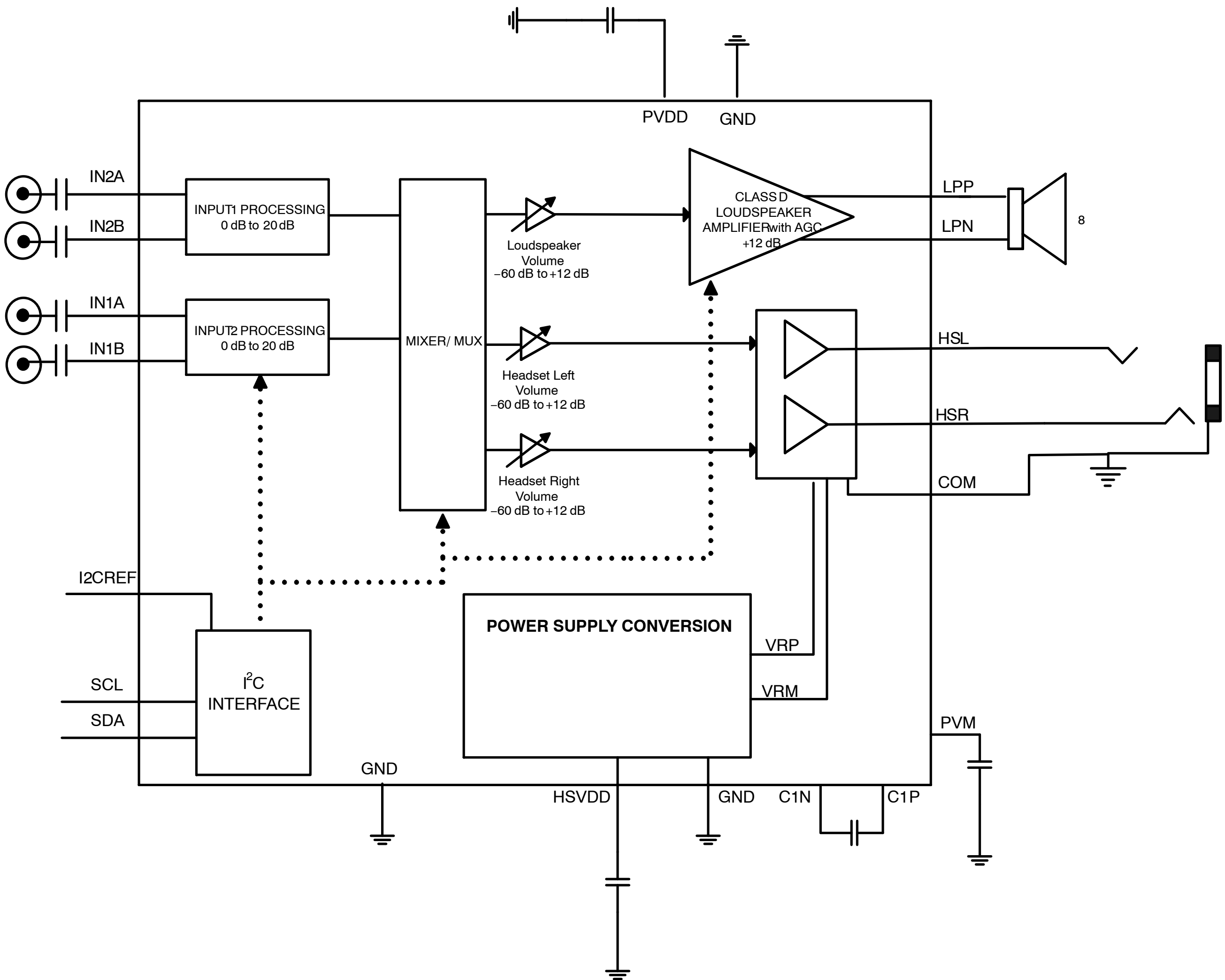


Figure 1. Simplified Block Diagram

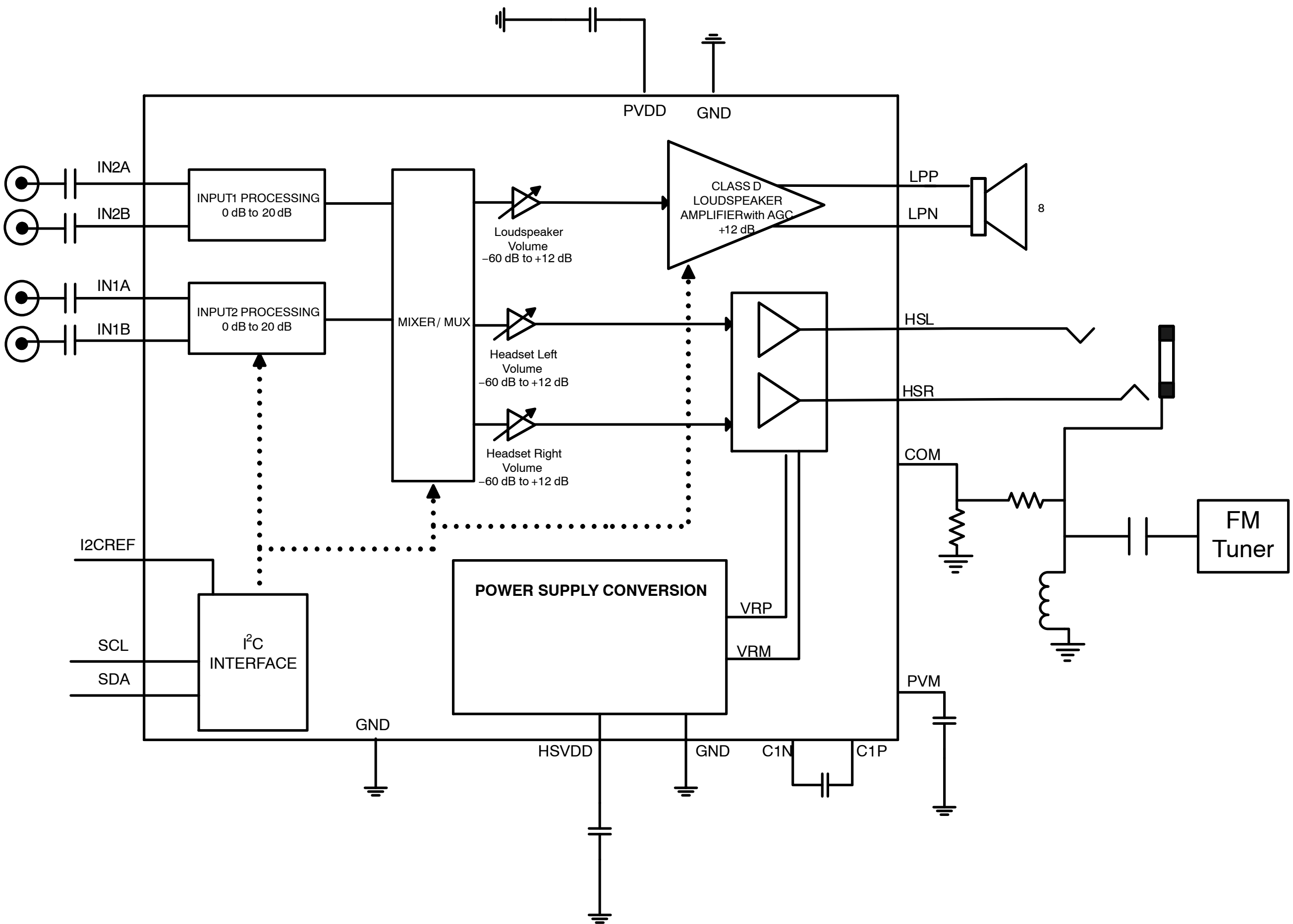


Figure 2. Simplified Block Diagram with FM radio antenna function

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
B2	IN1A	Input	First audio input. It is paired with IN1B. This pin is configured for single ended or differential type of input, pending on the I^2C programming.
A2	IN1B	Input	First audio input. It is paired with IN1A. This pin is configured for single ended or differential type of input, pending on the I^2C programming.
B1	IN2A	Input	Second audio input. It is paired with IN2B. This pin is configured for single ended or differential type of input, pending on the I^2C programming.
A1	IN2B	Input	Second audio input. It is paired with IN2A. This pin is configured for single ended or differential type of input, pending on the I^2C programming.
C3	SCL	Input	Clock input for the I^2C bus.
C4	SDA	Input / Output	Data input for the I^2C bus.
B3	GND	Power	Analog ground.
D4	HSV_{DD}	Power	Power supply dedicated to the charge pump and the headset amplifier. A low ESR ceramic capacitor to ground is required.
C5	GND	Power	Power ground dedicated to the charge pump and the headset amplifier.
C2	GND	Power	Power ground dedicated to the loudspeaker and the receiver.
A3	HSR	Output	Headset amplifier right output.
A4	HSL	Output	Headset amplifier left output.
B4	COM	Power	Ground reference for headphone amplifier
D1	LPN	Output	Loudspeaker negative output.
D3	LPP	Output	Loudspeaker positive output.
D2	PV_{DD}	Power	Power supply. A low ESR ceramic capacitor to ground is required.
C1	I^2CREF	Input	I2C reference voltage pin
D5	C1P	Output	Charge pump flying capacitor positive capacitor.
B5	C1N	Output	Charge pump flying capacitor negative capacitor.
A5	PVM	Output	Charge pump output. This is the symmetrical voltage of the power supply applied on the $HSV_{BAT.}$ A low ESR ceramic capacitor to ground is required.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
PV_{DD} : Power Supply Voltage (Note 1)	V_{IN}	−0.3 to +6.0	V
HSV_{DD} (Note 1)	V_{IN}	−0.3 to +4.5	V
Other Pins (Note 1)	V_{YY}	−0.3 to V_P +0.3	V
Human Body Model (HBM) ESD Rating are (Note 2)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 2)	ESD MM	200	V
CSP 2.5 x 2 mm package (Notes 6 and 7) Thermal Resistance Junction−to−Case	$R_{\theta JC}$	Note 7	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature (Note 6)	T_{JMAX}	+ 150	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	
Latchup Current	T_A	85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent of the PCB heat dissipation. The maximum power dissipation (P_D) is dependent by the min input voltage, the max output current and external components selected.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

ELECTRICAL CHARACTERISTICS Min & Max
Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for PV_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GENERAL						
PV_{DD}	Supply voltage range		2.5		5.5	V
HSV_{DD}	Supply voltage range		1.6		3.6	V
I^2CREF	I^2CREF voltage range		1.6		5.5	V
I_{SD}	Shutdown current	Soft shutdown at T_A = 25°C PV_{DD} HSV_{DD}		 0.1	 1	μA
I_Q	Quiescent current	Headset mode at T_A = 25°C, PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V PV_{DD} HSV_{DD} Speaker modeat T_A = 25°C, PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V PV_{DD} HSV_{DD} Headset + speaker modeat T_A = 25°C, PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V PV_{DD} HSV_{DD}		 0.1 2 2.2 1.8 2.2 2.8	 0.25 2.5 2.8 2.1 2.8 3.3	mA
R_{IN}	Input resistance		14	20	26	kΩ
R_{I2CREF}	I^2CREF pin pull−down resistance			100		kΩ
	Maximum input signal swing	Preamp = 0 dB, HSV_{DD} = 1.8 V, V_{LDO} = 1.6 V		1		V_{rms}
CMRR	Common mode rejection ratio	F = 1 kHz, differential input mode		−80		dB
T_{SD}	Thermal shutdown temperature			160		°C
T_{SD_hyst}	Thermal shutdown temperature hysteresis			20		°C
UVLO1	Undervoltage lockout on PV_{DD}	Falling edge		2.2		V
$UVLO1_{hys}$	UVLO hysteresis on PV_{DD}			150		mV
UVLO2	Undervoltage lockout on HSV_{DD}	Falling edge		1.4		V
$UVLO2_{hys}$	UVLO hysteresis on HSV_{DD}			100		mV
VOLUME CONTROL						
	Digital volume range Loudspeaker	Minimum gain Maximum gain		−60 12		dB
	Digital volume range Headset	Minimum gain Maximum gain		−60 12		dB
	Preamp gain	Input 1 or 2 INxG = 00 INxG = 01 INxG = 10 INxG = 11		 0 +6 +12 +20		dB
	Maximum gain setting Headset	INxG = 11 and gain control = 110100		+32		dB

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

ELECTRICAL CHARACTERISTICS Min & Max
Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for PV_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOLUME CONTROL						
	Maximum gain setting Speaker	INxG = 11 and gain control = 100111 (speaker amplifier has a gain of +12 dB)		+44		dB
LOUDSPEAKER						
$\lvert V_{OS} \rvert$	Absolute Offset Voltage	Inputs AC Grounded		±1		mV
$R_{DS(ON)}$	Static drain−source on−state resistance for both P and NMOS			200	300	mΩ
Z_{SD}	Output Impedance in Shutdown Mode			20		kΩ
I_{BR}	Current Breaker Threshold			2		A
F_{SW1}	Class D Switching Frequency			300		kHz
T_{ON}	Turn On Time			4		ms
T_{OFF}	Turn Off Time	No audio signal and outputs tied to GND		8		ms
P_O	RMS Output Power	R_L = 8 Ω, F = 1 kHz, THD+N < 1% PV_{DD} = 2.5 V PV_{DD} = 3.0 V PV_{DD} = 3.6 V PV_{DD} = 4.2 V PV_{DD} = 5.0 V		 0.33 0.49 0.71 0.97 1.4		W
P_O	RMS Output Power	R_L = 8 Ω, F = 1 kHz, THD+N < 10% PV_{DD} = 2.5 V PV_{DD} = 3.0 V PV_{DD} = 3.6 V PV_{DD} = 4.2 V PV_{DD} = 5.0 V		 0.41 0.60 0.87 1.20 1.7		W
THD+N	Total Harmonic Distortion + Noise	PV_{DD} = 5.0 V, P_{OUT} = 1 W, R_L = 8 Ω PV_{DD} = 3.6 V, P_{OUT} = 0.35 W, R_L = 8 Ω		0.1 0.1		%
SNR	Signal to Noise Ratio	PV_{DD} = 3.6 V, P_{OUT} = 0.8 W, R_L = 8 Ω		94		dB
CMRR	Common Mode Rejection Ratio	V_{ic} = 0.5 V to (V_{DD} – 0.8 V) R_L = 8 Ω, V_{ripple_pk-pk} F = 20 Hz to 20 kHz		−80		dB
PSRR	Power Supply Rejection Ratio	$V_{P\ ripple\_pk-pk}$ = 200 mV, R_L = 8 Ω Inputs AC grounded F = 217 Hz, Gain = 0 dB		−80		dB
η	Efficiency	R_L = 8 Ω, F = 1 kHz PV_{DD} = 3.6V, P_{OUT} = 0.6 W		87		%
HEADSET						
V_{OS}	Output offset voltage	Input AC grounded		± 1		mV
T_{WU}	Turning On time	Slow = 1 Slow = 0		1 34		ms
V_{LP}	Max Output Swing (peak value) (output in phase) (see LDO programming table, ≤ HSV_{DD} – 200 mV)	HSV_{DD} = 1.8 V, Headset = 16 Ω HSV_{DD} = 2.5 V, Headset = 16 Ω HSV_{DD} = 1.8 V, Headset = 32 Ω HSV_{DD} = 2.7 V, Headset = 32 Ω HSV_{DD} = 1.8 V, No load HSV_{DD} = 2.7 V, No load		1 1.65 1.3 2 1.6 2.5		V_{peak}

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

ELECTRICAL CHARACTERISTICS Min & Max
Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for PV_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HEADSET						
P_O	Max Output Power	HSV_{DD} = 1.8 V, THD+N = 1% Headset = 16 Ω Headset = 32 Ω		 30 26		mW
P_O	Max Output Power	HSV_{DD} = 2.5 V, THD+N = 1% Headset = 16 Ω Headset = 32 Ω		 86 62		mW
	Crosstalk	F = 1 kHz, P_{out} = 20 mW		−75		dB
PSRR	Power Supply Rejection Ratio	Inputs Shorted to Ground Gain = 0 dB F = 217 Hz to 1 kHz		−100		dB
THD+N	Total Harmonic Distortion + Noise	Headset = 16 Ω P_{OUT} = 15 mW, F = 1 kHz		0.015		%
THD+N	Total Harmonic Distortion + Noise	Headset = 32 Ω V_{OUT} = 400 mV, F = 1 kHz		−75		dB
C_{OUT}	Maximum Output Capacitance to Ground			100		pF
Z_{SD}	Output Impedance in Shutdown Mode			25		kΩ
F_{SW2}	Headset charge pump switching frequency	P_O > 500 μW		1.2		MHz
F_{SW3}	Headset charge pump switching frequency	P_O < 500 μW		150		kHz
SNR	Signal to Noise Ratio	HSV_{DD} = 1.8 V, P_{OUT} = 20 mW, R_L = 16 Ω		97		dB
V_{POP_HS}	Maximum Absolute Transient Voltage During Turn On and Off sequences	Input AC Grounded, A−Weighted filter, Volume = Mute		−70		dBV
I²C INTERFACE AND TIMING (Note 8)						
V_{IL}	Low input voltage level		−0.5		0.3 * I²CREF	V
V_{IH}	High input voltage level		0.7 * I²CREF		I²CREF + 0.5	V
V_{OL}	Low level output voltage		0		0.2 * I²CREF	V
$F_{CLK-MAX}$	Clock maximum speed		400			kHz
$t_{HD-START}$	Hold time (repeated) start condition		0.6			μs
t_{LOW}	Low period of SCL clock		1.3			μs
t_{HIGH}	High period of SCL clock		0.6			μs
$t_{SU-START}$	Setup time for a repeated start condition		0.6			μs
t_{SU-STO}	Setup time for STOP condition		0.6			μs
t_p	Power delay between PVDD and HSVDD		0			μs

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

ELECTRICAL CHARACTERISTICS Min & Max

Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for PV_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and PV_{DD} = 3.6 V, HSV_{DD} = 1.8 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I^2C INTERFACE AND TIMING (Note 8)						
t_{sw1}	Delay between PVDD and I^2C interface ready		300			μs
t_{sw2}	Delay between HSVDD and I^2C interface ready		300			μs
t_{en}	Delay between I^2CREF and I^2C communication		0			μs

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

TYPICAL OPERATING CHARACTERISTICS – LOUDSPEAKER

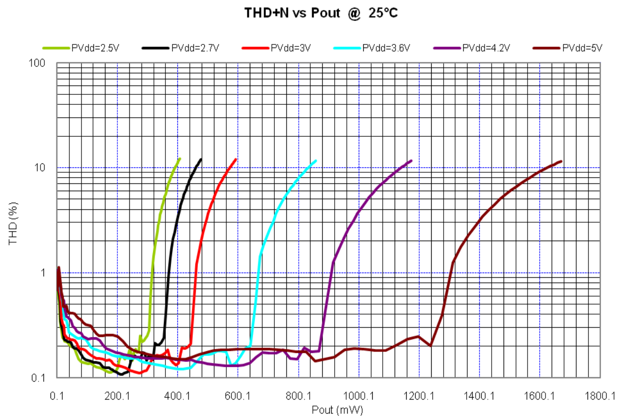


Figure 3. THD+N vs P_{out}, 8 Ω Load

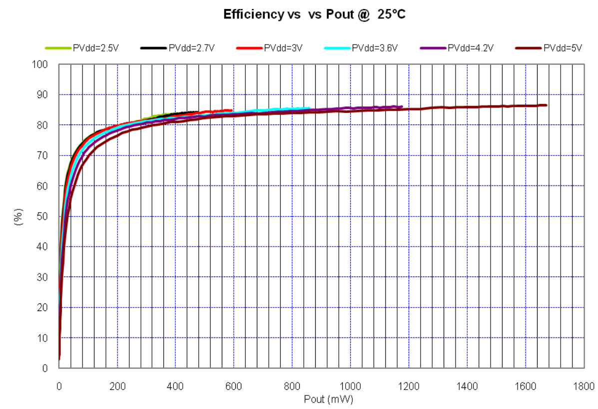


Figure 4. Efficiency vs P_{out}

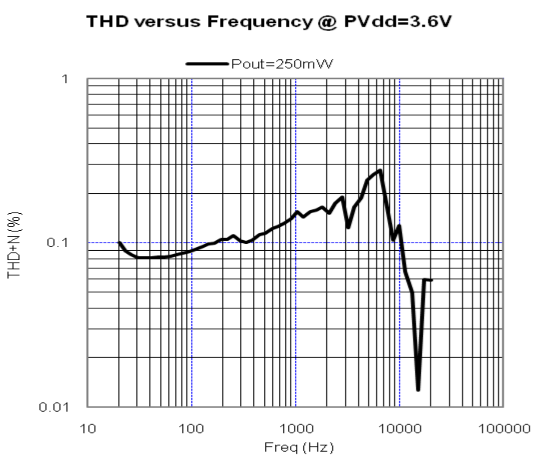


Figure 5. THD+N vs Frequency at PVDD = 3.6 V

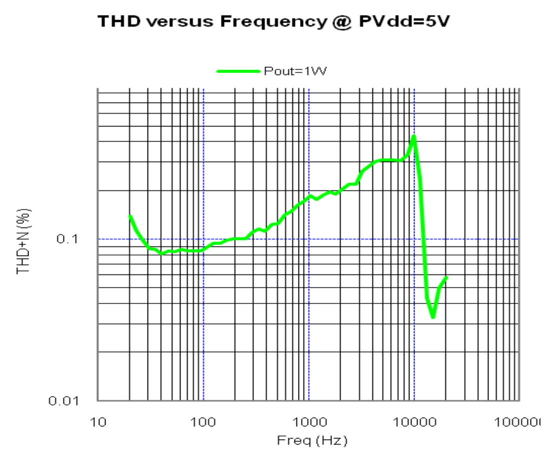


Figure 6. THD+N vs Frequency at PVDD = 5 V

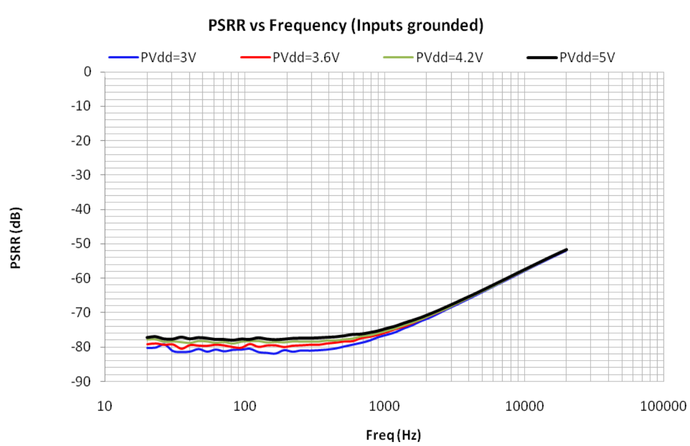


Figure 7. PSRR vs Frequency

TYPICAL OPERATING CHARACTERISTICS – HEADPHONE

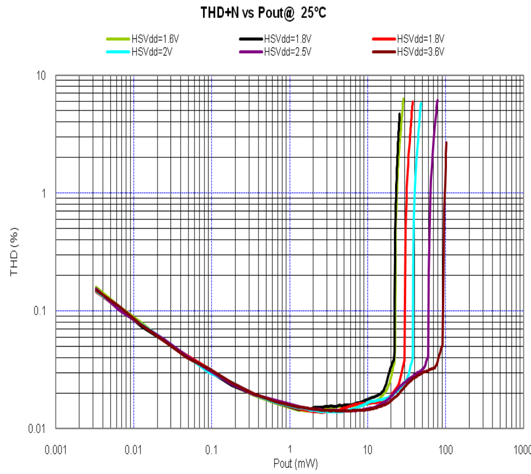


Figure 8. THD+N vs P_{out}, 32 Ω Load in Phase

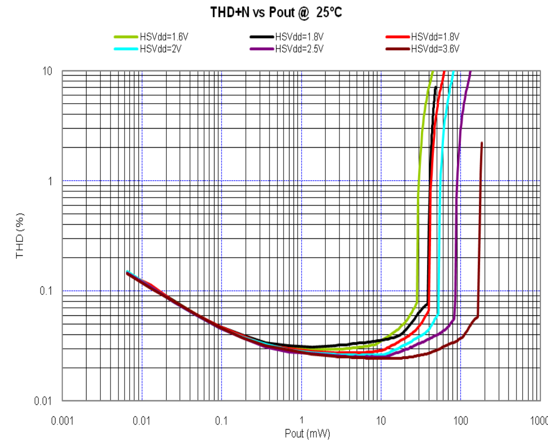


Figure 9. THD+N vs P_{out}, 16 Ω Load in Phase

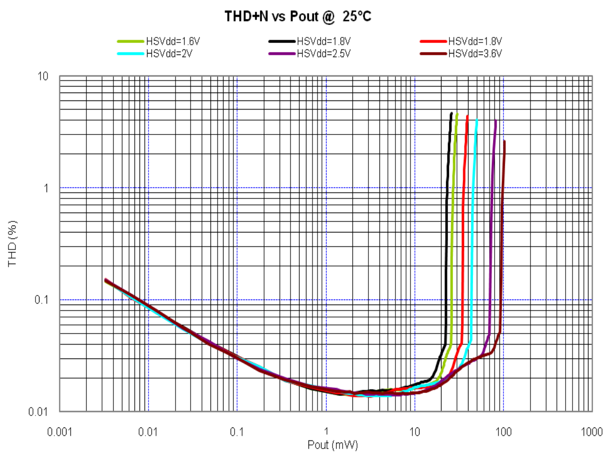


Figure 10. THD+N vs P_{out}, 32 Ω Load Out of Phase

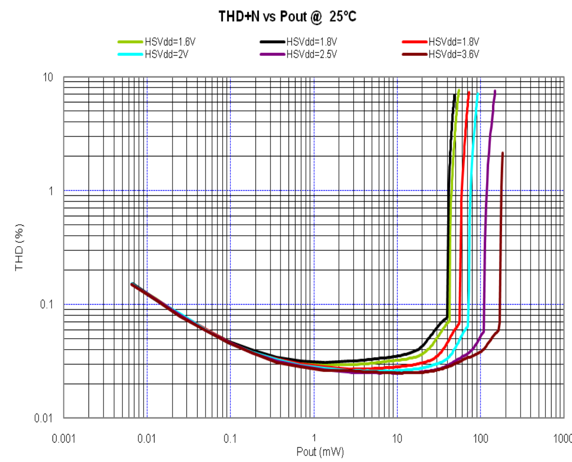


Figure 11. THD+N vs P_{out}, 16 Ω Load Out of Phase

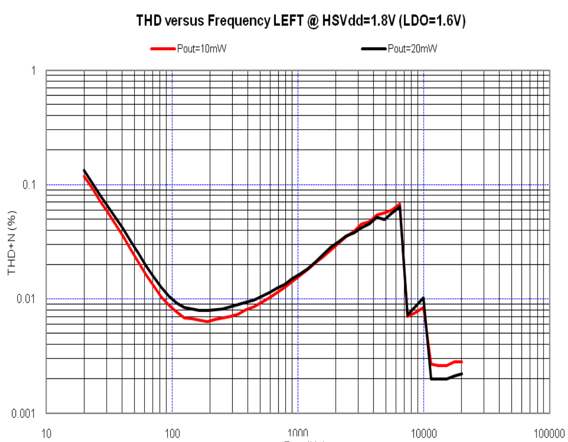


Figure 12. THD+N vs Frequency, 32 Ω Load in Phase, Left Channel

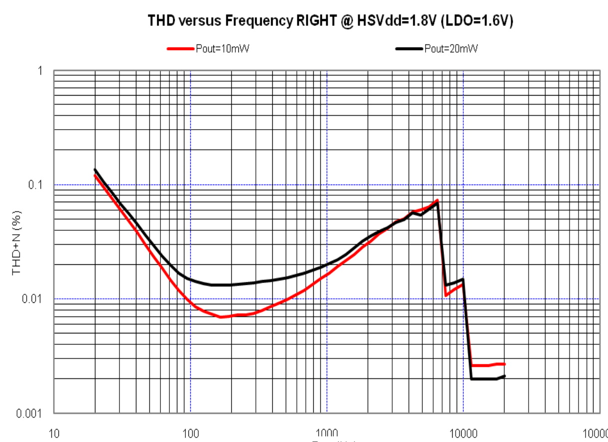


Figure 13. THD+N vs Frequency, 32 Ω Load in Phase, Right Channel

TYPICAL OPERATING CHARACTERISTICS – HEADPHONE

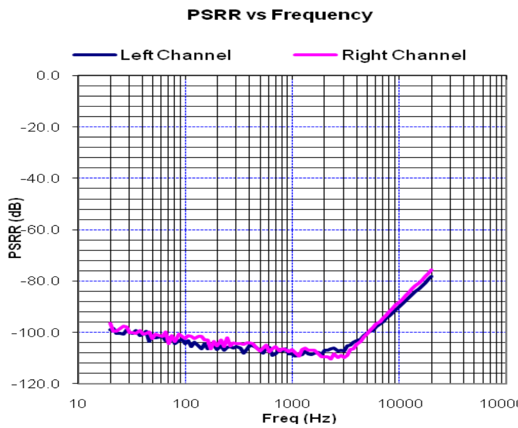


Figure 14. PSRR vs Frequency

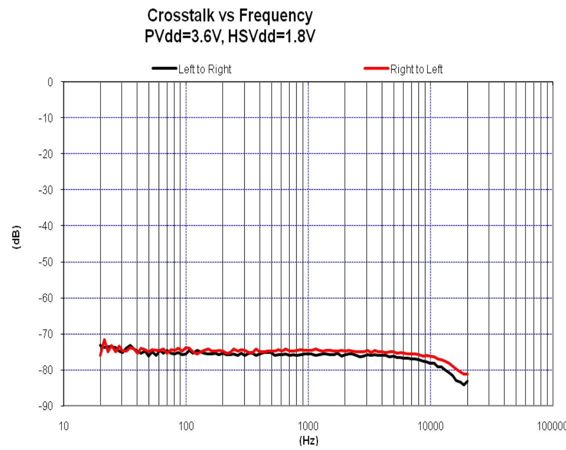


Figure 15. Crosstalk vs Frequency

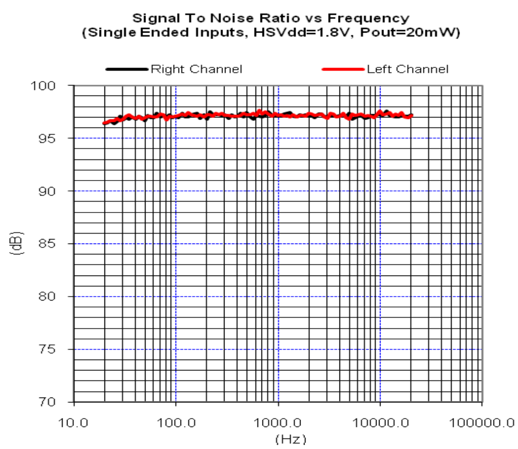


Figure 16. SNR vs Frequency at Pout = 20 mW

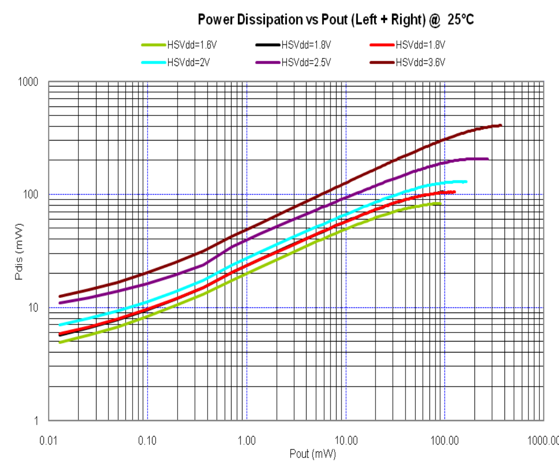


Figure 17. Power Dissipation vs P_{out} with 16 Ω Load

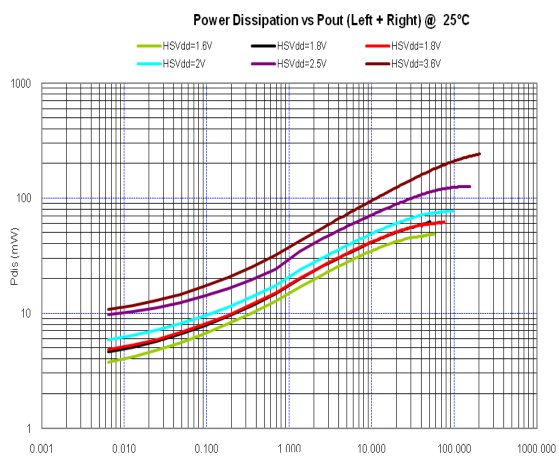


Figure 18. Power Dissipation vs P_{out} with 32 Ω Load

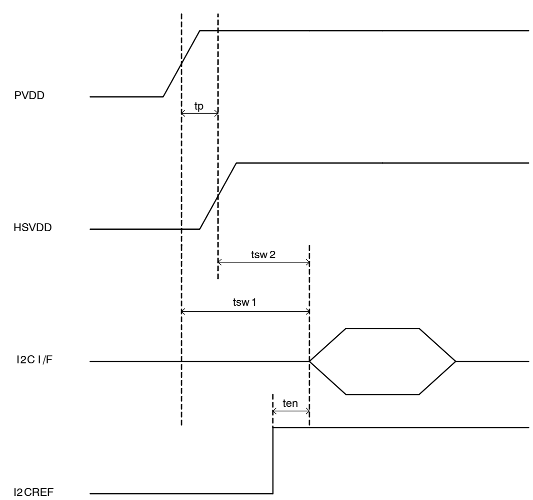


Figure 19. Supply Voltage Timing

DETAIL OPERATING DESCRIPTION

DETAILED DESCRIPTIONS

I^2C COMPATIBLE INTERFACE

Start and Stop Conditions

Communication is initiated by HIGH to LOW transition on SDA line while SCL is still high. This signal configuration defines the START condition (noted S). Communication is terminated when a LOW to HIGH transition occurs on SDA while SCL is high. This defines the STOP condition (noted P).

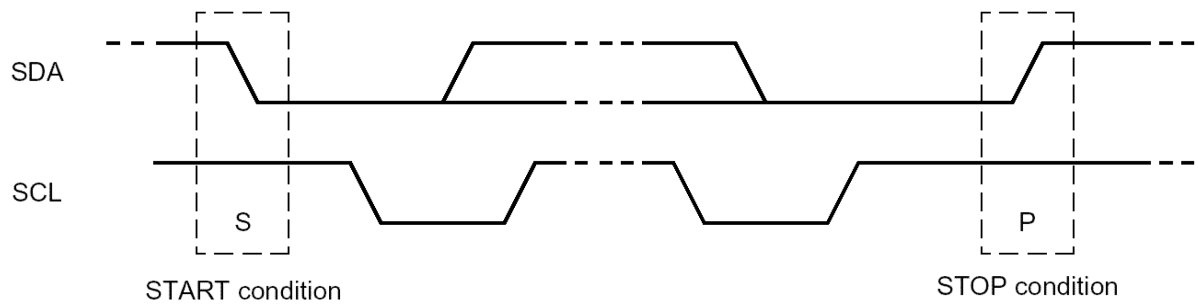


Figure 20. Start and Stop Bits Configuration on the I^2C Bus

Data Validity

During normal data transmission, the SDA will not transition during a SCL High.

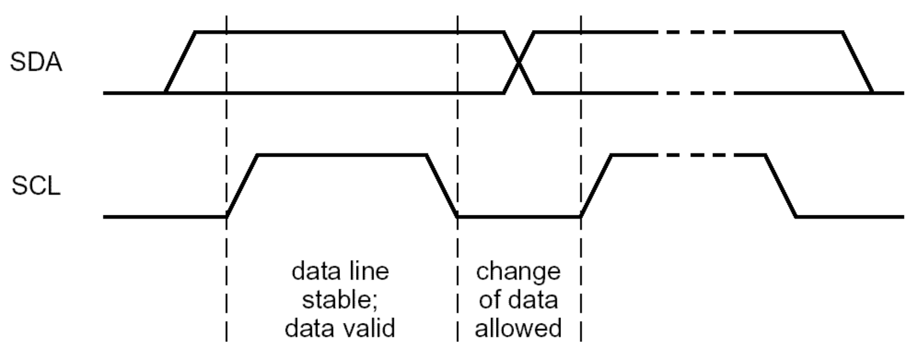


Figure 21. Data Validity

Data Transfer on the I^2C Bus

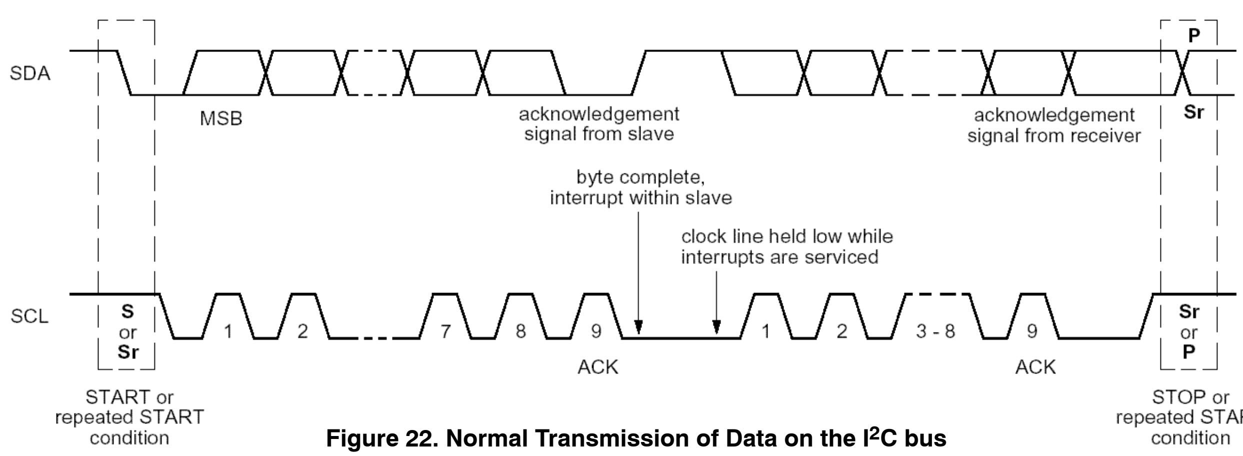


Figure 22. Normal Transmission of Data on the I^2C bus

Data communication begins with a Start. The first transmitted Byte is the Slave address (7 bits, MSB first) followed by the Read/Write bit. A "zero" indicates a "write" and a "one" indicates a "read" sequence. The byte is followed by an acknowledgement (mandatory) where the receiver pulls down the SDA line after the last received bit, to indicate that the information was received correctly. The receiver releases the SDA line after the 9th SCL pulse. Then the second byte may be transmitted.

More details about Data transfer and Acknowledgement may be found in Chapter 7 of "the I^{2}C bus specification".

Note about "repeated Start" (Sr)

A Sr condition can happen any time during an I2C transaction. The SDA line cannot transition while SCL line is in High level state, except for START / STOP and Sr conditions. A Sr condition is a equivalent to a START condition (SDA line transitions from High to Low while SCL is High level). However, a STOP condition is not necessary before a Start. When there is no Stop, the Start is called Sr:

Normal STOP Then START:

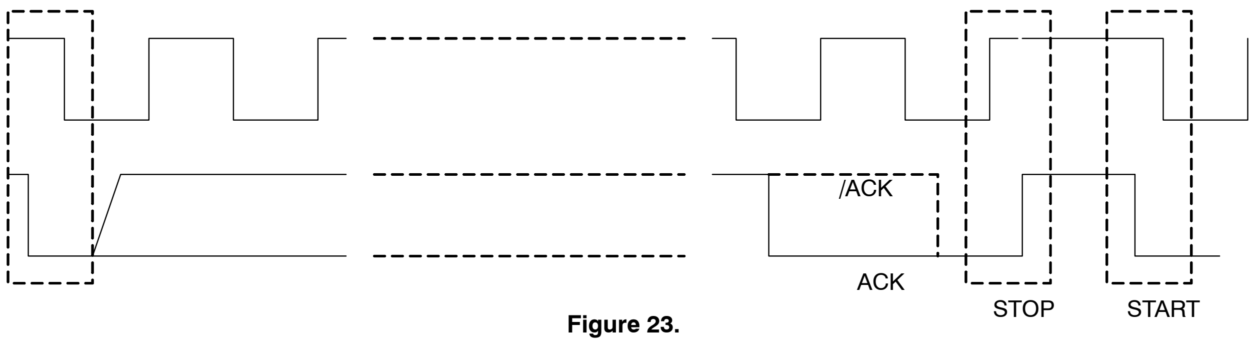


Figure 23.

Repeated Start (Sr):

First case: SDA transitions normally from 0 to 1 during SCL low state. However, master generates a Start during SCL high state. This is a Start without stop and is a Sr condition

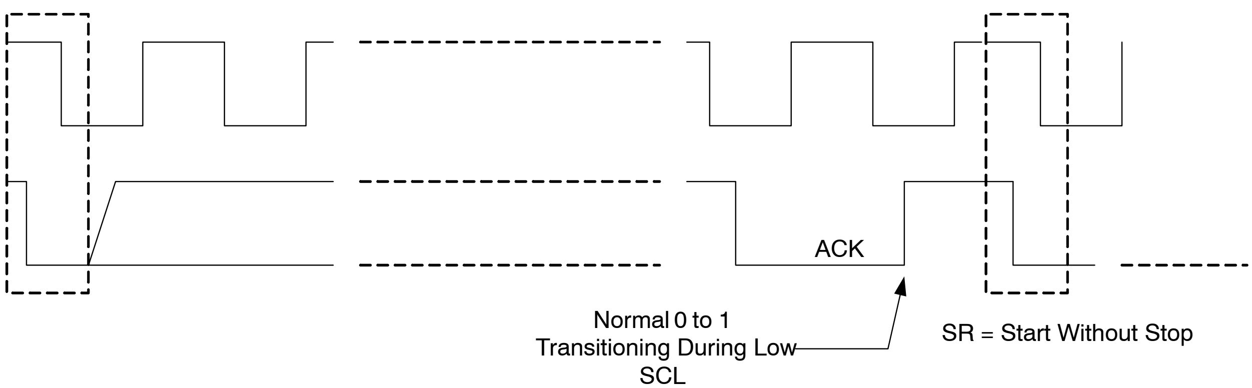


Figure 24.

Second case: SDA is already at High state (for example after a /ACK. Then, master generates a Start during SCL high state. This is a Start without stop and is a Sr condition.

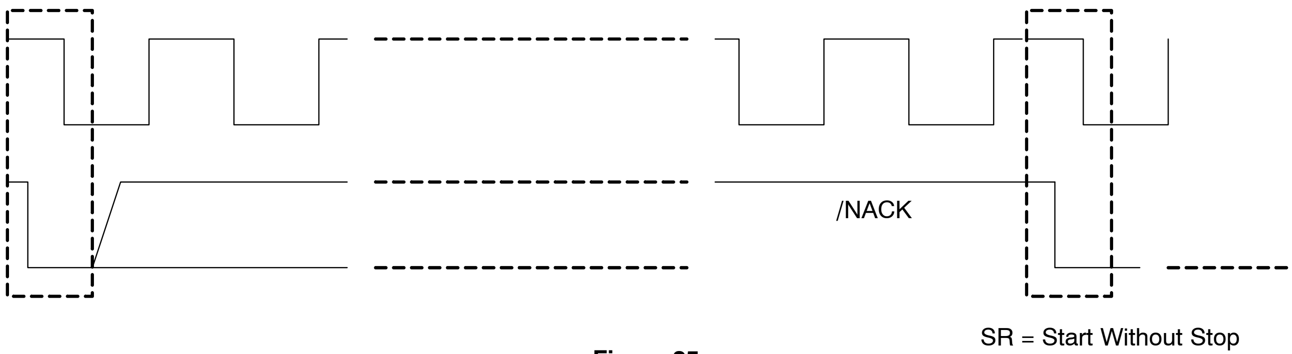


Figure 25.

Bus Timing

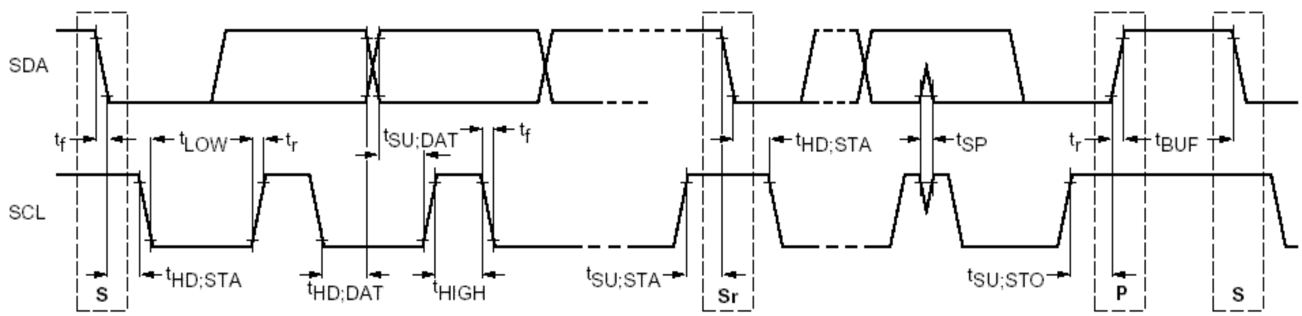


Figure 26.

NCP2705 I2C ADDRESS

I^2C Address							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	0	0	0	0	1	X

REGISTER MAP

12 different registers can be addressed through the “Register Address” byte.

Register Number	Function	I^{2}C Address							
		D7	D6	D5	D4	D3	D2	D1	D0
0	Input Control	–	–	0	0	0	0	0	0
1	Speaker Volume Control	–	–	0	0	0	0	0	1
2	Left Volume Control	–	–	0	0	0	0	1	0
3	Right Volume Control	–	–	0	0	0	0	1	1
4	Output control	–	–	0	0	0	1	0	0
5	LDO Control	–	–	0	0	0	1	0	1
6	Status	–	–	0	0	0	1	1	0
7	ACNT	–	–	0	0	0	1	1	1
8	ACONFA	–	–	0	0	1	0	0	0
9	ACONFR	–	–	0	0	1	0	0	1
10	ACONFH	–	–	0	0	1	0	1	0
11	EMI control	–	–	0	0	1	0	1	1
59	Reserved*	–	–	1	1	1	0	1	1
60	Reserved*	–	–	1	1	1	1	0	0
61	Reserved*	–	–	1	1	1	1	0	1
62	Reserved*	–	–	1	1	1	1	1	0
63	Reserved*	–	–	1	1	1	1	1	1

*End user should never neither read nor write this register

INPUT CONTROL

This register allows the setting of the input stage as follows:

INxC sets up the configuration on each input. NCP2705 brings the flexibility to set up each input pair for a differential input signal or two single−ended ones.

− 1 = Inputs are set as differential input with InxA as the positive and InxB as the negative.

− 0 = Inputs are set as stereo single−ended input with InxA as left input and InxB as right input.

D7	D6	D5	D4	D3	D2	D1	D0
x	x	IN1C	IN2C	IN1G		IN2G	

IN1G configures the gain on the first input

D3	D2	IN1G
0	0	0 dB
0	1	+ 6 dB
1	0	+ 12 dB
1	1	+ 20 dB

IN2G configures the gain on the second input

D1.	D0	IN2G
0	0	0 dB
0	1	+ 6 dB
1	0	+ 12 dB
1	1	+ 20 dB

When a single−ended configuration is required, for example a stereo signal, the first internal stage is described on **Figure 27**:

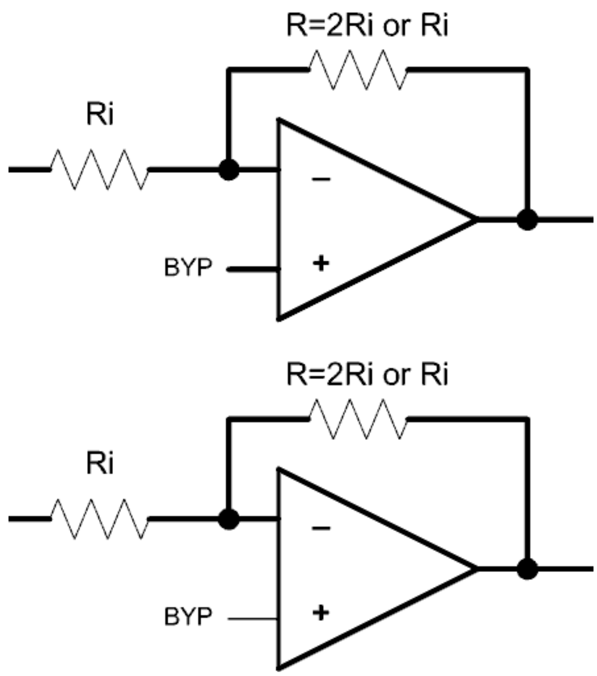


Figure 27. NCP2705 Input Stage for Single Ended Type of Input

When a differential audio signal is used, the internal first stage is described in **Figure 28**:

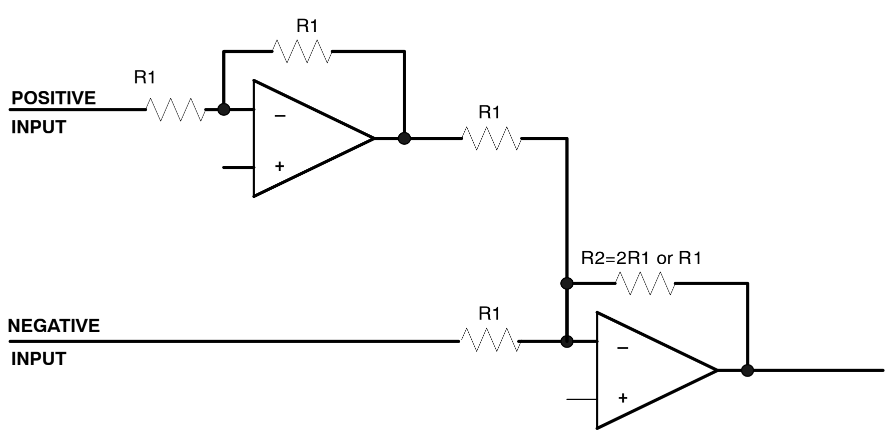


Figure 28. NCP2705 Input Stage for Differential type of Input

RIGHT, LEFT VOLUME CONTROL

As described in the register "**REGISTER MAP**" section, NCP2705 allows separated volume control for Headset Right, Headset Left.

D7**	D6**	D5	D4	D3	D2	D1	D0
x	x	GAIN CONTROL					

**D7 and D6 bits can be either 0 or 1. NCP2705 will only process D5 to D0 to address the targeted gain setting.

D5	D4	D3	D2	D1	D0	Gain (dB)
0	0	0	0	0	0	Mute
0	0	0	0	0	1	−60
0	0	0	0	1	0	−54
0	0	0	0	1	1	−48
0	0	0	1	0	0	−45
0	0	0	1	0	1	−42
0	0	0	1	1	0	−39
0	0	0	1	1	1	−36
0	0	1	0	0	0	−34
0	0	1	0	0	1	−32
0	0	1	0	1	0	−30
0	0	1	0	1	1	−28
0	0	1	1	0	0	−27
0	0	1	1	0	1	−26
0	0	1	1	1	0	−25
0	0	1	1	1	1	−24
0	1	0	0	0	0	−23
0	1	0	0	0	1	−22
0	1	0	0	1	0	−21
0	1	0	0	1	1	−20
0	1	0	1	0	0	−19
0	1	0	1	0	1	−18
0	1	0	1	1	0	−17
0	1	0	1	1	1	−16
0	1	1	0	0	0	−15
0	1	1	0	0	1	−14
0	1	1	0	1	0	−13
0	1	1	0	1	1	−12
0	1	1	1	0	0	−11
0	1	1	1	0	1	−10
0	1	1	1	1	0	−9
0	1	1	1	1	1	−8
1	0	0	0	0	0	−7
1	0	0	0	0	1	−6
1	0	0	0	1	0	−5
1	0	0	0	1	1	−4
1	0	0	1	0	0	−3

D5	D4	D3	D2	D1	D0	Gain (dB)
1	0	0	1	0	1	−2
1	0	0	1	1	0	−1
1	0	0	1	1	1	0
1	0	1	0	0	0	+1
1	0	1	0	0	1	+2
1	0	1	0	1	0	+3
1	0	1	0	1	1	+4
1	0	1	1	0	0	+5
1	0	1	1	0	1	+6
1	0	1	1	1	0	+7
1	0	1	1	1	1	+8
1	1	0	0	0	0	+9
1	1	0	0	0	1	+10
1	1	0	0	1	0	+11
1	1	0	0	1	1	+12

As described above, an additional gain setting is possible in the “**INPUT CONTROL**” register. Thus, final gain setting can go up to **32 dB** for the signal applied on the IN1 and IN2 input.

SPEAKER VOLUME CONTROL

As described in the register “**REGISTER MAP**” section, NCP2705 allows separated volume control for Loudspeaker.

D7***	D6***	D5	D4	D3	D2	D1	D0
x	x	DIGITAL GAIN CONTROL					

***D7 and D6 bits can be either 0 or 1. NCP2705 will only process D5 to D0 to address the targeted gain setting.

D5	D4	D3	D2	D1	D0	Gain (dB)
0	0	0	0	0	0	Mute
0	0	0	0	0	1	−60
0	0	0	0	1	0	−54
0	0	0	0	1	1	−48
0	0	0	1	0	0	−45
0	0	0	1	0	1	−42
0	0	0	1	1	0	−39
0	0	0	1	1	1	−36
0	0	1	0	0	0	−34
0	0	1	0	0	1	−32
0	0	1	0	1	0	−30
0	0	1	0	1	1	−28
0	0	1	1	0	0	−27
0	0	1	1	0	1	−26
0	0	1	1	1	0	−25
0	0	1	1	1	1	−24
0	1	0	0	0	0	−23
0	1	0	0	0	1	−22
0	1	0	0	1	0	−21

D5	D4	D3	D2	D1	D0	Gain (dB)
0	1	0	0	1	1	−20
0	1	0	1	0	0	−19
0	1	0	1	0	1	−18
0	1	0	1	1	0	−17
0	1	0	1	1	1	−16
0	1	1	0	0	0	−15
0	1	1	0	0	1	−14
0	1	1	0	1	0	−13
0	1	1	0	1	1	−12
0	1	1	1	0	0	−11
0	1	1	1	0	1	−10
0	1	1	1	1	0	−9
0	1	1	1	1	1	−8
1	0	0	0	0	0	−7
1	0	0	0	0	1	−6
1	0	0	0	1	0	−5
1	0	0	0	1	1	−4
1	0	0	1	0	0	−3
1	0	0	1	0	1	−2
1	0	0	1	1	0	−1
1	0	0	1	1	1	0
1	0	1	0	0	0	+1
1	0	1	0	0	1	+2
1	0	1	0	1	0	+3
1	0	1	0	1	1	+4
1	0	1	1	0	0	+5
1	0	1	1	0	1	+6
1	0	1	1	1	0	+7
1	0	1	1	1	1	+8
1	1	0	0	0	0	+9
1	1	0	0	0	1	+10
1	1	0	0	1	0	+11
1	1	0	0	1	1	+12

As described above, an additional gain setting is possible in the “**INPUT CONTROL**” register. Thus, final gain setting can go up to **44 dB** for the signal applied on the IN1 and IN2 input.

OUTPUT CONTROL

The NCP2705 embeds one class D loudspeaker amplifier and a true ground headset stereo amplifier (Left and Right). The "**INPUT CONTROL**" register has defined the Input 1 and 2 configuration (single−ended or differential). The last stage of the audio subsystem defines which between IN1A, IN1B, IN2A, IN2B or a combination is applied to each amplifier.

D7	D6	D5	D4	D3	D2	D1	D0
x	Reset	/SD	Slow	Output Mode			

POWER ON RESET CONDITIONS

D6	RESET
0	No I^2C Register Change
1	I^2C Register in Reset Configuration

The **RESET** function can be set by driving D6 bit to high Level. In that case, all registers are set in the following configuration.

Registers	Reset configuration							
	D7	D6	D5	D4	D3	D2	D1	D0
Input control	0	0	0	0	0	0	0	0
Headset right volume control	0	0	0	0	0	0	0	0
Headset left volume control	0	0	0	0	0	0	0	0
Loudspeaker volume control	0	0	0	0	0	0	0	0
Output control	0	0	x	0	0	0	0	0
LDO control	0	0	0	0	0	0	0	0
Status	0	0	0	0	0	0	0	1
AGC control register	0	0	1	1	1	1	1	1
AGC configuration register Attack time	0	0	0	0	0	0	0	1
AGC configuration register Release time	0	0	0	0	0	0	0	1
AGC configuration register Hold time	0	0	0	0	0	0	0	0
EMI control	0	0	0	0	0	0	0	0

Reset Functionality and Default State

Reset configuration will be effective in 3 different application cases:

- **POR**: As soon as power supply is detected by NCP2705, all the registers are set in the default configuration.
- **RESET bit**: It can be done in the Mode control register by setting D6 bit (RESET) to 1. Then Mode Control and Gain Control registers are set in their default state. Once done, RESET bit goes back to 0. Reset can be done independently the state of the /SD bit.
- **RESET Threshold**:
  - When PV_{DD} decreases and goes below UVLO threshold (2.2 V), the amplifiers enter in shutdown mode. When PV_{DD} goes over UVLO + Hysteresis the amplifiers turn on with the previous configuration.
  - When HSV_{DD} decreases and goes below UVLO threshold (1.3 V), the amplifiers enter in shutdown mode. When HSV_{DD} goes over UVLO + Hysteresis the amplifiers turn on with the previous configuration.

Shutdown functionality

NCP2705 has an internal software shutdown through bit D5 of the Output control register.

- **Software Shutdown**: When a software shutdown occurs through D5 bit in the "Output control" register (D5 = 0), the device enter in a low power shutdown mode.
- **Output configuration**

Conf N°	OUTPUT MODE 0				OUTPUT CONFIGURATION with IN1C = IN2C = 0		
	D3	D2	D1	D0	Loudspeaker	Left Headset	Right Headset
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	IN1A + IN1B	SD	SD
2	0	0	1	0	SD	IN1A	IN1B
3	0	0	1	1	IN1A + IN1B	IN1A	IN1B
4	0	1	0	0	IN2A + IN2B	SD	SD
5	0	1	0	1	SD	IN2A	IN2B
6	0	1	1	0	IN2A + IN2B	IN2A	IN2B
7	0	1	1	1	IN1A + IN1B + IN2A + IN2B	SD	SD
8	1	0	0	0	SD	IN1A + IN2A	IN1B + IN2B
9	1	0	0	1	IN1A + IN1B + IN2A + IN2B	IN1A + IN2A	IN1B + IN2B
10	1	0	1	0	IN1A + IN1B	IN2A	IN2B
11	1	0	1	1	IN2A + IN2B	IN1A	IN1B
12	1	1	0	0	SD	SD	SD
13	1	1	0	1	SD	SD	SD
14	1	1	1	0	SD	SD	SD
15	1	1	1	1	SD	SD	SD

Conf N°	OUTPUT MODE 1				OUTPUT CONFIGURATION with IN1C = IN2C = 1		
	D3	D2	D1	D0	Loudspeaker	Left Headset	Right Headset
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	IN1_Diff	SD	SD
2	0	0	1	0	SD	IN1_Diff	IN1_Diff
3	0	0	1	1	IN1_Diff	IN1_Diff	IN1_Diff
4	0	1	0	0	IN2_Diff	SD	SD
5	0	1	0	1	SD	IN2_Diff	IN2_Diff
6	0	1	1	0	IN2_Diff	IN2_Diff	IN2_Diff
7	0	1	1	1	IN1_Diff + IN2_Diff	SD	SD
8	1	0	0	0	SD	IN1_Diff + IN2_Diff	IN1_Diff + IN2_Diff
9	1	0	0	1	IN1_Diff + IN2_Diff	IN1_Diff + IN2_Diff	IN1_Diff + IN2_Diff
10	1	0	1	0	IN1_Diff	IN2_Diff	IN2_Diff
11	1	0	1	1	IN2_Diff	IN1_Diff	IN1_Diff
12	1	1	0	0	SD	SD	SD
13	1	1	0	1	SD	SD	SD
14	1	1	1	0	SD	SD	SD
15	1	1	1	1	SD	SD	SD

Conf N°	OUTPUT MODE 2				OUTPUT CONFIGURATION with IN1C = 1 and IN2C = 0		
	D3	D2	D1	D0	Loudspeaker	Left Headset	Right Headset
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	IN1_Diff	SD	SD
2	0	0	1	0	SD	IN1_Diff	IN1_Diff
3	0	0	1	1	IN1_Diff	IN1_Diff	IN1_Diff
4	0	1	0	0	IN2A + IN2B	SD	SD
5	0	1	0	1	SD	IN2A	IN2B
6	0	1	1	0	IN2A + IN2B	IN2A	IN2B
7	0	1	1	1	SD	SD	SD
8	1	0	0	0	SD	SD	SD
9	1	0	0	1	SD	SD	SD
10	1	0	1	0	IN1_Diff	IN2A	IN2B
11	1	0	1	1	IN2A + IN2B	IN1_Diff	IN1_Diff
12	1	1	0	0	SD	SD	SD
13	1	1	0	1	SD	SD	SD
14	1	1	1	0	SD	SD	SD
15	1	1	1	1	SD	SD	SD

Conf N°	OUTPUT MODE 3				OUTPUT CONFIGURATION with IN1C = 0 and IN2C = 1		
	D3	D2	D1	D0	Loudspeaker	Left Headset	Right Headset
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	IN1A + IN1B	SD	SD
2	0	0	1	0	SD	IN1A	IN1B
3	0	0	1	1	IN1A + IN1B	IN1A	IN1B
4	0	1	0	0	IN2_Diff	SD	SD
5	0	1	0	1	SD	IN2_Diff	IN2_Diff
6	0	1	1	0	IN2_Diff	IN2_Diff	IN2_Diff
7	0	1	1	1	SD	SD	SD
8	1	0	0	0	SD	SD	SD
9	1	0	0	1	SD	SD	SD
10	1	0	1	0	IN1A + IN1B	IN2_Diff	IN2_Diff
11	1	0	1	1	IN2_Diff	IN1A	IN1B
12	1	1	0	0	SD	SD	SD
13	1	1	0	1	SD	SD	SD
14	1	1	1	0	SD	SD	SD
15	1	1	1	1	SD	SD	SD

AGC CONTROL

The AGC function is to protect the speaker from damage due to exceeded output power. The function limits the output power without deteriorating the audio quality.

AGC CONTROL REGISTER (ACNT)

This register allows controlling the AGC setup.

D7	D6	D5	D4	D3	D2	D1	D0	
AGCE	NC/L	PWR(2)	PWR(1)	PWR(0)	THD(2)	THD(1)	THD(0)	ACNT

THD(2−0) : Define the maximum distortion level acceptable in non−clipping mode.

THD Bit	Maximum THDN Level
000	1%
001	2%
010	4%
011	6%
100	8%
101	10%
110	15%
111	20%

PWR(2−0) : Define the maximum peak voltage in output of the amplifier in case of limiter mode.

PWR Bit	$V_{peakmax}$ (V)
000	0.5
001	1
010	1.5
011	2
100	2.5
101	3
110	3.5
111	4

NC/L : Non−clipping mode and limiter mode selection bit.

- 0 = Non−clipping mode.
- 1 = Limiter mode.

AGCE : Activate or disable the AGC function bit.

- 0 = AGC disable.
- 1 = AGC enable.

AGC CONFIGURATION REGISTER (ACONFA−ACONFR−ACONFH)

This register controls the AGC configuration.

D7*	D6*	D5	D4	D3	D2	D1	D0	
x	x	A(5)	A(4)	A(3)	A(2)	A(1)	A(0)	ACONFA
x	x	R(5)	R(4)	R(3)	R(2)	R(1)	R(0)	ACONFR
x	x	H(5)	H(4)	H(3)	H(2)	H(1)	H(0)	ACONFH

A(5−0) : Define the attack time.

A(5−0)	ms/0.5dB	ms/6dB
00000	Class D clock	
00001	0.1067	1.28
00010	0.2134	2.56
00011	0.3201	3.84
−−−	0.1067 ms/step	−−−
11111	6.722	80.66

Attack time is defined as the minimum time between two gain decrease.

R(5−0) : Define the release time.

R(5−0)	s/0.5dB	s/6dB
00000	Class D clock	
00001	0.0137	0.1644
00010	0.0274	0.3288
00011	0.0411	0.4932
−−−	0.0137s/step	−−−
11111	0.8631	10.36

Release time is defined as the minimum time between two gain increase.

H(5−0) : Define the hold time.

H(5−0)	Timer Hold (s)
00000	Hold time off
00001	0.0137
00010	0.0274
00011	0.0411
−−−	0.0137s/step
11111	0.8631

Hold time is defined as the minimum time between a gain increase after a gain decrease.

EMI CONTROL

The EMI control register set the rising and falling edges of the Class D speaker outputs. This register gives the possibility to the user to have the best efficiency by choosing the lowest value, or reduce the EMI perturbation by increasing it. By default the programming value set the fastest time to have the best efficiency.

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	EMI Control			

D3	D2	D1	D0	Value tr and tf (ns)
0	0	0	0	20
0	0	0	1	15
0	0	1	0	10
0	0	1	1	5
0	1	0	0	1
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

HEADSET SUPPLY VOLTAGE AND LDO SETTING

- Apply a supply voltage from 1.6 V to 3.6 V to the pin HSV_{DD}. The internal signal VRP and VRM will be the output of an internal converter set by the LDO control register.
- HSV_{DD} must be ≥ $V_{LDO\ SETTING}$ + 200 mV.

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	Internal LDO Output			

The LDO control register bits (D3 to D0) set VRP and VRM.

D3	D2	D1	D0	Internal LDO Output V_{peak}
0	0	0	0	1.3
0	0	0	1	1.4
0	0	1	0	1.5
0	0	1	1	1.6
0	1	0	0	1.7
0	1	0	1	1.8
0	1	1	0	1.9
0	1	1	1	2.0
1	0	0	0	2.1
1	0	0	1	2.2
1	0	1	0	2.3
1	0	1	1	2.4
1	1	0	0	2.5
1	1	0	1	2.6
1	1	1	0	2.7
1	1	1	1	2.8

This function helps to increase the output dynamic when external damping resistors are used.
Maximum input signal swing is linked to $V_{LDO\ SETTING}$.

Internal LDO Output V_{peak}	Maximum input signal swing V_{PP}
1.3	2.6
1.4	2.8
1.5	3.0
1.6	3.2
1.7	3.4
1.8	3.6
1.9	3.8
2.0	4.0
2.1	4.2
2.2	4.4
2.3	4.6
2.4	4.8
2.5	5.0
2.6	5.2
2.7	5.4
2.8	5.6

STATUS REGISTER

This register gives the status of the fault which can occur in the NCP2705.

D7	D6	D5	D4	D3	D2	D1	D0
x	x	WSLDO	SC_LPP	SC_LPN	SC_HSL	SC_HSR	HSVDD

D0: This bit indicates if HSVDD is present (D0 = 0) or not (D0 = 1).

D1: This bit indicates that the current limitation of the pin HSR is activated (D1 = 1). It is automatically reset to 0 when the fault disappears.

D2: This bit indicates that the current limitation of the pin HSL is activated (D2 = 1). It is automatically reset to 0 when the fault disappears.

D3: This bit indicates that the current limitation of the pin LPN is activated (D3 = 1). It is automatically reset to 0 when the fault disappears.

D4: This bit indicates that the current limitation of the pin LPP is activated (D4 = 1). It is automatically reset to 0 when the fault disappears.

D5: This bit indicates that a wrong setting on the LDO control register has been done. This fault occurs when LDO setting > HSV_{DD} – 200 mV. It is automatically reset to 0 when the fault disappears.

Components Selection

Input Capacitor Selection

The input coupling capacitor blocs the DC voltage at the amplifier input. This capacitor creates a high−pass filter with R_{in} (20 kΩ).

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation in the audio bandwith (20 Hz – 20 kHz).

The cut off frequency for the input high−pass filter is : $F_c = 1 / (2\pi R_{in} C_{in})$.

Charge Pump Capacitor Selection

Use ceramic capacitor with low ESR for better performances. X5R / X7R capacitor is recommended.

The flying capacitor serves to transfer charge during the generation of the negative voltage. Connect CFly as closed as possible of C1P and C1M.

The PVM capacitor must be equal at least to the CFly capacitor to allow maximum transfer charge. Connect CPVM as closed as possible of the PVM pin.
A value of 1 μF is recommended.

The following table suggests typical value and manufacturer:

Value	Reference	Package	Manufacturer
1 μF	C1005X5R0J105K	0402	TDK
1 μF	GRM155R60J105K16	0402	Murata

Lower value of capacitors can be used but the maximum output power is reduced and the device may not operate to specifications.

Long Play True Ground Headphone Power Supply Decoupling Capacitor

The headphone amplifier requires the adequate decoupling capacitor in order to guarantee the best operation in terms of audio performances. Use X5R / X7R ceramic capacitor and place it closed to the HSVDD pin. A value of 1 μF is recommended.

Class D Power Supply Decoupling Capacitor

The Class D amplifier requires the adequate decoupling amplifier in order to guarantee the best operation in terms of audio performances. Use X5R / X7R ceramic capacitor and place it closed to PVDD pin in order to reduce high frequency transient spikes due to parasitic inductance. A value of 4.7 μF is recommended.

Layout Recommendations

For efficiency, noise and EMI standpoints, it is strongly recommended to use Power and ground plane in order to reduce parasitic resistance and inductance.

For the same reason, it is strongly recommended for the class D amplifier to keep the output traces short and well shielded in order to avoid them to act as antenna.

Route audio signal (input pins and HSL / HSR) far from HSVDD, C1P, C1M, PVM, PVDD, LPP, and LPN to avoid any perturbation due to the switching.

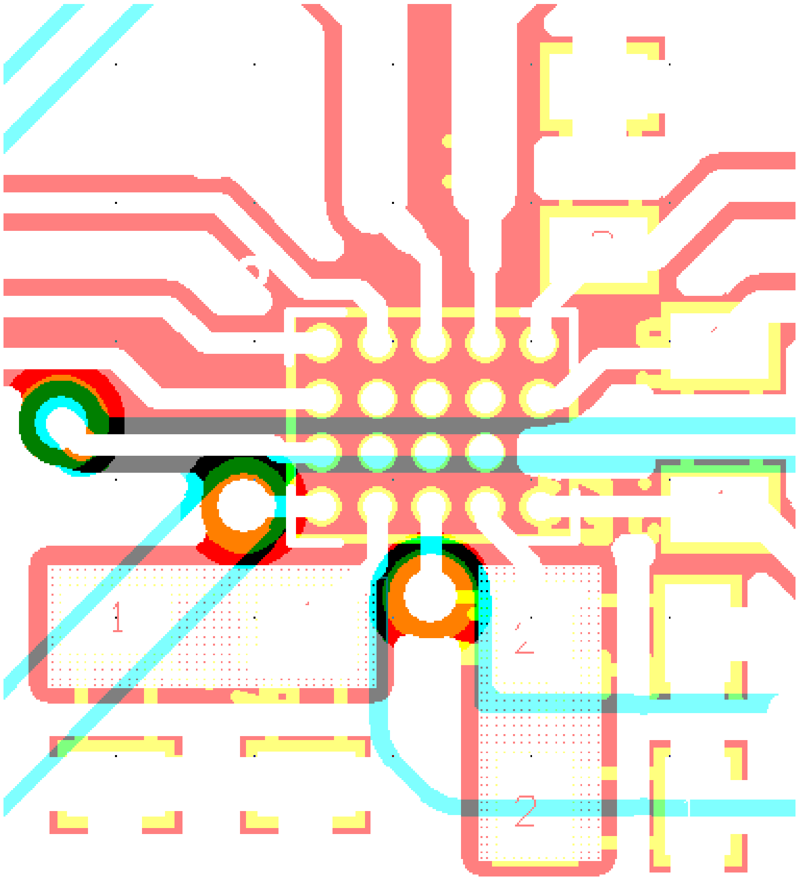


Figure 29. PCB Layout Example

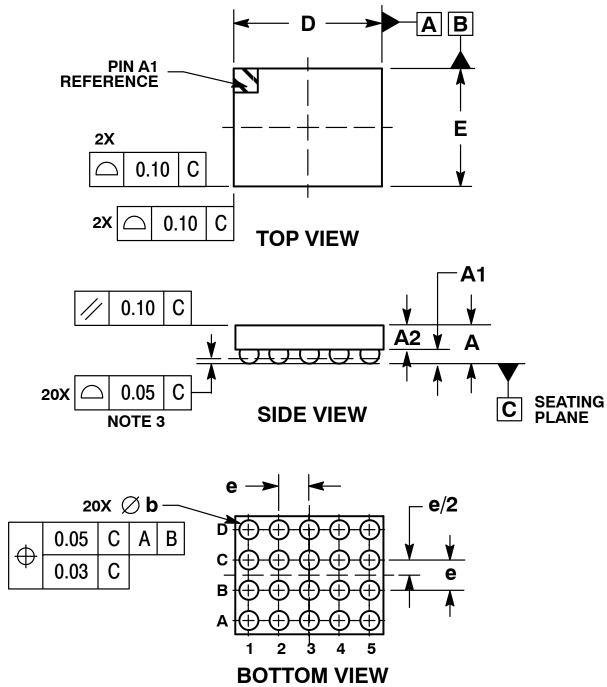
ORDERING INFORMATION

Device	Package	Shipping†
NCP2705FCCT1G	CSP – 20 – 2.5 x 2.0 mm (Backside Laminate Coating) (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

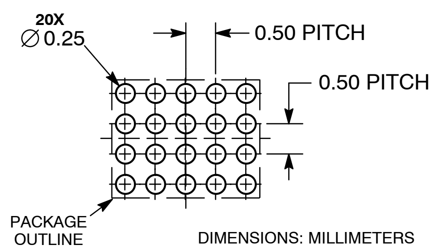
20 PIN FLIP−CHIP, 2.5x2.0, 0.5P
CASE 499BH−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. DIE COAT, 0.04 THICK, PERMISSABLE ON THIS SURFACE. DIE COAT THICKNESS IS INCLUDED IN DIMENSIONS A AND A2.

	MILLIMETERS	
DIM	MIN	MAX
A	0.54	0.66
A1	---	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.50 BSC	
E	2.00 BSC	
e	0.50 BSC	

RECOMMENDED SOLDER FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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